



Specifications

- Die Thickness
- Gold Wire
- Pd/Cu Wire
- Ag Wire
- Mold Cap Thickness
- Marking
- Packing Options

Reliability

- Moisture Sensitivity Level
  - JEDEC Level 2A, 260°C Reflow
- Temperature Cycling
  - Condition C (–65°C to 150°C), 1000 cycles
- High Temperature Storage
  - 150°C, 1000 hrs
- Pressure Cooker Test
  - 121°C, 100% RH/2 atm, 168 hrs
- Temperature/Humidity Test
  - 85°C/85% RH, 1000 hrs
- Unbiased HAST
  - 130°C/85% RH/2 atm, 96 hrs

Thermal Performance  $\theta_{ja}$  (°C/W)

| Package | Body Size (mm) | Pin Count | Die Size (mm) | Thermal Performance $\theta_{ja}$ (C/W) |
|---------|----------------|-----------|---------------|-----------------------------------------|
| LFBGA   | 11 x 11 (2L)   | 144       | 4.5 x 4.5     | 34.1                                    |
| LFBGA   | 15 x 15 (4L)   | 208       | 10.2 x 10.2   | 19.4                                    |

Note: Simulation data for package mounted on 4 layer PCB (per JEDEC JESD51-7) under natural convection as defined in JESD51-2.

| Conductor Component | Length (mm) | Resistance (mOhms) | Inductance (nH) | Inductance Mutual (nH) | Capacitance (pF) | Capacitance Mutual (pF) |
|---------------------|-------------|--------------------|-----------------|------------------------|------------------|-------------------------|
| Wire                | 2           | 120                | 1.65            | 0.45 - 0.85            | 0.10             | 0.01 - 0.02             |
| Net (2L)            | 2 - 7       | 34 - 119           | 1.30 - 4.55     | 0.26 - 2.28            | 0.25 - 0.95      | 0.06 - 0.42             |
| Net (4L)            | 4 - 9       | 154 - 239          | 2.95 - 6.20     | 0.71 - 3.13            | 0.35 - 1.05      | 0.07 - 0.44             |
| Wire                | 2           | 120                | 1.65            | 0.45 - 0.85            | 0.10             | 0.01 - 0.02             |
| Net (4L)            | 2 - 7       | 34 - 119           | 0.90 - 3.15     | 0.18 - 1.582           |                  |                         |
|                     |             |                    |                 |                        |                  |                         |

Cross Sections

FPGA

